

Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1. (Currently amended) A programmable processor comprising:
 - an instruction path;
 - a data path;
 - an external interface operable to receive data from an external source and communicate the received data over the data path;
 - a register file operable to receive and store data from the data path and communicate the stored data to the data path; and
 - an execution unit coupled to the instruction and data paths and operable to decode and execute instructions received from the instruction path, wherein in response to decoding a single instruction for writing data to memory based on a mask and data contained in at least one register specifying both a mask and a register containing data, the mask comprising fields that each correspond to a field of the data contained in the at least one register, the execution unit is operable to:
 - (i) detect some of the fields of the mask as having a predetermined value ~~and identifying to identify~~ corresponding fields of the data contained in the at least one register as write-enabled data fields; and
 - (ii) cause the write-enabled data fields to be written to a specified memory location.

2. (Original) The processor of claim 1 wherein each of the fields of the mask has a width of one bit.

3. (Currently amended) The processor of claim 1 wherein each of the fields of the data contained in the at least one register has a width of one bit.

4. (Original) The processor of claim 1 wherein the execution unit is operable to cause the write-enabled data fields to be written to the specified memory location by reading an unaltered field of data from the specified memory location and writing the unaltered field of data along with the write-enabled data fields to the specified memory location.

5. (Original) The processor of claim 1 wherein the mask is contained in a specified register.

6. (Currently amended) The processor of claim 1 wherein the memory location is ~~contained in a specified~~ specified by a register.

7. (Original) The processor of claim 1 wherein the specified memory location comprises a section of memory having a specific width and beginning at a specific memory address.

8. (Original) The processor of claim 1 wherein the predetermined value is a logic 1.

9. (Currently amended) The processor of claim 1 wherein the execution unit is further operable to, in response to decoding a second single instruction specifying a ~~third and a fourth~~ register ~~each~~ containing a first plurality of floating-point operands and another register containing a second plurality of floating-point operands, multiply the first plurality of floating

~~point floating-point~~ operands ~~in the third register~~ by the second plurality of floating-point operands ~~in the fourth register~~ to produce a plurality of products and provide the plurality of products to partitioned fields of a result register as a ~~second~~ catenated result.

10. (Currently amended) A data processing system comprising:

- (a) a bus coupling components in the data processing system;
- (b) an external memory coupled to the bus;
- (c) a programmable microprocessor coupled to the bus and capable of operation

independent of another host processor, the microprocessor comprising:

an instruction path; a data path;

an external interface operable to receive data from an external source and communicate the received data over the data path;

a register file operable to receive and store data from the data path and communicate the stored data to the data path; and

an execution unit coupled to the instruction and data paths and operable to decode and execute instructions received from the instruction path, wherein in response to decoding a single instruction for writing data to memory based on a mask and data contained in at least one register ~~specifying both a mask and a register containing data~~, the mask comprising fields that each correspond to a field of the data contained in the at least one register, the execution unit is operable to:

(i) detect some of the fields of the mask as having a predetermined value ~~and~~
~~identifying to identify~~ corresponding fields of the data contained in the at least one register as
write-enabled data fields; and

(ii) cause the write-enabled data fields to be written to a specified memory
location.

11. (Original) The system of claim 10 wherein each of the fields of the mask has a width
of one bit.

12. (Currently amended) The system of claim 10 wherein each of the fields of the data
contained in the at least one register has a width of one bit.

13. (Original) The system of claim 10 wherein the execution unit is operable to cause
the write-enabled data fields to be written to the specified memory location by reading an
unaltered field of data from the specified memory location and writing the unaltered field of data
along with the write-enabled data fields to the specified memory location.

14. (Original) The system of claim 10 wherein the mask is contained in a specified
register.

15. (Currently amended) The system of claim 10 wherein the memory location is
~~contained in a specified~~ specified by a register.

16. (Original) The system of claim 10 wherein the specified memory location comprises
a section of memory having a specific width and beginning at a specific memory address.

17. (Original) The system of claim 10 wherein the predetermined value is a logic 1.

18. (Currently amended) The system of claim 10 wherein the execution unit is further operable to, in response to decoding a second single instruction specifying a ~~third and a fourth~~ register each containing a first plurality of floating-point operands and another register containing a second plurality of floating-point operands, multiply the first plurality of ~~floating point~~ floating-point operands ~~in the third register~~ by the second plurality of floating-point operands ~~in the fourth register~~ to produce a plurality of products and provide the plurality of products to partitioned fields of a result register as a ~~second~~ catenated result.

19. (Currently amended) A programmable processor comprising:

a virtual memory addressing unit;

an instruction path and a data path;

an external interface operable to receive data from an external source and communicate the received data over the data path;

a cache operable to retain data communicated between the external interface and the data path;

a register file comprising a plurality of registers coupled to the data path; and an execution unit, coupled to the instruction and data paths, that is operable to decode and execute instructions received from the instruction path, the execution unit capable of performing a bitwise insert operation that operates on a first and a second operand stored in at least one

register registers in the register file, wherein for each bit in the first operand, the bitwise insert operation inserts the bit into a corresponding bit position in a destination value if a corresponding bit from the second operand has a first predetermined value.

20. (Previously presented) The programmable processor of claim 19 wherein the first predetermined value is a logic 1.

21. (Previously presented) The programmable processor of claim 19 wherein for each bit in the first operand, the bitwise insert operation maintains a corresponding bit position in the destination value as unchanged if a corresponding bit in the second operand has a second predetermined value.

22. (Previously presented) The programmable processor of claim 21 wherein the second predetermined value is a logic 0.

23. (Previously presented) The programmable processor of claim 19 wherein the bitwise insert operation stores the destination value into memory.

24. (Previously presented) The programmable processor of claim 19 wherein each of the first and second operands has a width of 64 bits.

25. (Currently amended) The programmable processor of claim 19 wherein the execution unit is further capable of executing a plurality of different group floating-point arithmetic operations that arithmetically operate on multiple floating-point operands stored in

partitioned fields of ~~an operand register~~ registers in the register file ~~plurality of registers~~ to produce a catenated result that is returned to a register in the register file ~~plurality of registers~~, wherein the catenated result comprises a plurality of individual floating-point results.

26. (Currently amended) A device having installed therein a programmable processor, the programmable processor comprising:

a virtual memory addressing unit;

an instruction path and a data path;

an external interface operable to receive data from an external source and communicate the received data over the data path;

a cache operable to retain data communicated between the external interface and the data path;

a register file comprising a plurality of registers coupled to the data path; and an execution unit, coupled to the instruction and data paths, that is operable to decode and execute instructions received from the instruction path, the execution unit capable of performing a bitwise insert operation that operates on a first and a second operand stored in at least one register ~~registers~~ in the register file, wherein for each bit in the first operand, the bitwise insert operation inserts the bit into a corresponding bit position in a destination value if a corresponding bit from the second operand has a first predetermined value.

27. (Previously presented) The device of claim 26 wherein the first predetermined value is a logic 1.

28. (Previously presented) The device of claim 26 wherein for each bit in the first operand, the bitwise insert operation maintains a corresponding bit position in the destination value as unchanged if a corresponding bit in the second operand has a second predetermined value.

29. (Previously presented) The device of claim 28 wherein the second predetermined value is a logic 0.

30. (Previously presented) The device of claim 26 wherein the bitwise insert operation stores the destination value into memory.

31. (Previously presented) The device of claim 26 wherein each of the first and second operands has a width of 64 bits.

32. (Currently amended) The device of claim 26 wherein the execution unit is further capable of executing a plurality of different group floating-point arithmetic operations that arithmetically operate on multiple floating-point operands stored in partitioned fields of an operand register registers in the register file plurality of registers to produce a catenated result that is returned to a register in the register file plurality of registers, wherein the catenated result comprises a plurality of individual floating-point results.